Indium Gallium Arsenide Microwave Power Transistors

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Abstract—**Depletion-mode InGaAs microwave power MISFET's with 1 μm gate lengths and up to 1 mm gate widths have been fabricated using an ion-implanted process. The devices employed a plasma-deposited silicon/silicon dioxide gate insulator. The dc current–voltage (I–V) characteristics and RF power performance at 9.7 GHz are presented. The output power, power-added efficiency, and power gain as a function of input power are reported. An output power of 1.07 W at 9.7 GHz with a corresponding power gain and power-added efficiency of 4.3 dB and 38%, respectively, was obtained. The large-gate-width devices provided over twice the previously reported output power for InGaAs MISFET's at X band. In addition, the first report of RF output power stability of InGaAs MISFET's over a 24 h period is also presented. An output power stability within 1.2% over 24 h of continuous operation was achieved. In addition, a drain current drift of 4% over 10^4 s was obtained.**

I. Introduction

INDIUM gallium arsenide (InGaAs) is a promising electronic material for high-frequency applications. $In_{0.53}Ga_{0.47}As$ lattice matched to semi-insulating (SI) indium phosphide (InP) has higher low-field mobility (12000 cm^2/V s), peak electron velocity (3×10^7 cm/s), and intervalley separation (0.55 eV) than InP or gallium arsenide (GaAs) [1]. Because of the low Schottky barrier height of InGaAs, development of a metal–semiconductor field-effect transistor (MESFET) technology is not feasible. Consequently, much emphasis has been placed on the development of a metal–insulator–semiconductor field-effect transistor (MISFET) technology. A MISFET device structure provides a high input voltage swing, which is advantageous for power devices. Bipolar gate voltage swings are also possible, which provide improved linearity [2]. In addition, high gate breakdown voltages and low gate leakage currents are associated with the deposited gate insulator. Because of the above-mentioned materials properties, InGaAs MISFET's have potential for superior microwave performance compared with InP MISFET's. However, because InGaAs has lower ionization coefficients and a lower breakdown field than InP, high-frequency device operation may be attained at the expense of reduced power output.

N-channel inversion mode MISFET's first demonstrated the feasibility of a MISFET technology on InGaAs [3], [4]. These early devices were fabricated on p-InGaAs layers grown using liquid phase epitaxy (LPE), and employed plasma-deposited silicon dioxide and silicon nitride gate insulators. Depletion-mode InGaAs MISFET's were subsequently fabricated on n^+/n InGaAs layers grown using hydride vapor phase epitaxy (VPE) [5]. Devices with 3 μm gate lengths and silicon dioxide gate insulators had effective mobilities of 5200 cm^2/V s. Inversion-mode InGaAs MISFET's with native oxide gate insulators have also been reported [6], [7]. The devices were fabricated on epitaxial layers grown by molecular beam epitaxy (MBE). A transconductance of 40 mS/mm was obtained for devices with 3 μm gate lengths.

More recently, depletion-mode InGaAs MISFET's with 1 μm gate lengths have demonstrated a transconductance of 300 mS/mm [8]. The carrier velocity was estimated to be 4×10^7 cm/s. InGaAs MISFET's have also been fabricated on n^+/n layers grown by metal organic chemical vapor deposition (MOCVD) [9], [10]. Enhancement-mode devices with 1.5 μm gate lengths exhibited a transconductance of 300 mS/mm. The effective channel mobility and carrier velocity were determined to be 5800 cm^2/V s and 3.5×10^7 cm/s, respectively [10]. Depletion-mode InGaAs MISFET's with an ultrathin MBE silicon interfacial layer between the InGaAs and photo-CVD silicon dioxide gate insulator have recently demonstrated an effective channel mobility of 1700 cm^2/V s [11].

Depletion-mode InGaAs MISFET's with 3 μm gate lengths first demonstrated microwave power performance at 6 GHz [5]. Ion-implanted InGaAs MISFET's with 1 μm gate lengths have since demonstrated output power densities of 0.49 W/mm of gate width with corresponding power-added efficiencies of 48% and 39% at 4 GHz and 8 GHz, respectively [2]. InGaAs power MISFET's with 1 μm gate lengths have also been fabricated using a non-ion-implanted process [8]. Microwave performance was demonstrated in the frequency range from 4 GHz to 32.5 GHz. Output power densities obtained from devices with 0.56 mm gate widths were 1.53 W/mm, 0.76 W/mm, 0.74

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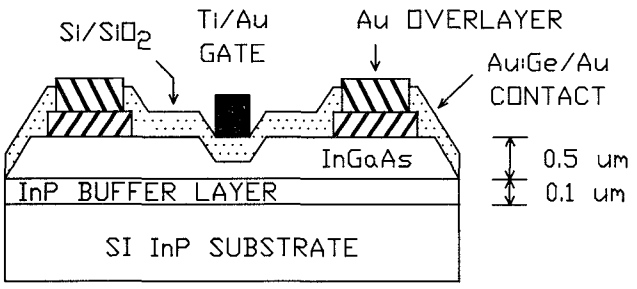

Fig. 1. Schematic representation of the cross section of an InGaAs MISFET with silicon/silicon dioxide gate insulator.

W/mm, and 0.20 W/mm at 4 GHz, 12 GHz, 20 GHz, and 32 GHz, respectively. The corresponding power-added efficiencies were 53%, 40%, 26%, and 7%. Recently, the wide-band microwave power performance of InGaAs MISFET amplifiers has been reported [12]. Output power densities of 0.41 W/mm and 0.47 W/mm with corresponding power-added efficiencies of $33\pm3\%$ and $30\pm3\%$, respectively, were obtained over the 7–11 GHz band. In addition, an output power density of 0.39 W/mm with $29\pm4\%$ power-added efficiency was obtained over the 6–12 GHz band.

In comparison with InGaAs MISFET's, InP MISFET's have recently demonstrated impressive output power densities. Ion-implanted InP MISFET's with 1 μm gate lengths have produced output power densities of 2.9 W/mm and 2.4 W/mm at X band [13], [14]. Epitaxial InP MISFET's with similar geometries have produced output power densities of 4.5 W/mm [15]. In addition, an epitaxial InP MISFET with a 0.3 μm gate length has achieved an output power density of 1.8 W/mm at Ka band [16].

This paper reports on the fabrication of 1-μm-gate-length, depletion-mode, high-power InGaAs MISFET's using an ion-implanted process. The device employed a plasma-deposited silicon/silicon dioxide gate insulator. The dc current–voltage (I–V) characteristics and RF power performance at 9.7 GHz are presented. The output power, power-added efficiency, and power gain as a function of input power are reported. For the first time, RF power results were obtained for InGaAs MISFET's with gate widths up to 1 mm.

II. Experimental

A schematic cross section of the 1-μm-gate-length InGaAs MISFET with a silicon/silicon dioxide gate insulator is shown in Fig. 1. The devices were fabricated on InGaAs layers grown lattice matched on semi-insulating (SI) InP substrates with resistivity greater than $10^7\ \Omega\cdot$cm. The thicknesses of the InGaAs layer and InP buffer layer were 0.5 μm and 0.1 μm, respectively. The ohmic contracts were Au:Ge/Au of 0.35 μm thickness, and the thickness of the Au overlayer was 0.4 μm. The gate metal was Ti/Au of 0.43 μm thickness. The source/drain implant spacing was 5 μm, and the length of the gate recess was 2 μm. The completed InGaAs MISFET's had six to ten parallel gate fingers with individual gate widths of 100 or 125 μm. The individual gate finger width was limited to the above values in order to avoid possible gain degradation associated with larger gate widths [14]. The total gate widths were 0.75, 0.8, or 1 mm. The average separation between the gate fingers was 114 μm. The large spacing between the gate fingers was necessary in order to facilitate wire bonding to the individual drain regions.

The InGaAs and InP layers were grown unintentionally doped ($n=1$–2×10^{15} cm^{-3}) on SI–InP substrates using metal-organic chemical vapor deposition (MOCVD) [17]. The SI–InP substrates were liquid encapsulated Czochralski (LEC) grown wafers 2 in. in diameter with (100) orientation. The substrates were cleaned using organic solvents and then etched using a H_2SO_4:H_2O_2:H_2O solution. The layers were deposited using a vertical, low-pressure (60 torr), rotating (1500 rpm) disk reactor with a 3–2 in. diameter wafer capacity (EMCORE GS/3200). The growth chamber is of stainless steel construction and contains a resistively heated molybdenum susceptor. The wafers rest directly on a wafer carrier which is transferred between an ultrahigh-vacuum stainless steel load lock and the heated susceptor in the growth chamber. The temperature is monitored by a thermocouple or infrared pyrometry.

The In and Ga metal-organic sources were trimethylindium (TMI) and triethylgallium (TEG). The As and P hydride sources were arsine (10% AsH_3/H_2) and phosphine (PH_3). Hydrogen was used as a carrier gas. A high-temperature bakeout was performed with temperatures of 650°–690°C for 15 min prior to growth. The growth rate for the InGaAs and InP layers was 1.9 μm/h. The growth temperature was 620°C. Typical values for InGaAs and InP thickness uniformity across a 2 in. wafer were $<\pm2\%$. The lattice mismatch variation was $<\pm10^{-4}$ across the 2 in. wafer. The InGaAs mobility at 300 K was 12000 cm^2/V s.

For the InGaAs MISFET fabrication, the samples were initially cleaned by first decreasing in acetone and methanol followed by a DI water rinse. The samples were then dipped for 15 s in a 10:1 H_2O:HF solution followed by a DI water rinse and then blown dry in nitrogen.

The cross section of the fabrication sequence of the InGaAs MISFET's is illustrated in Fig. 2. After the initial clean, the first photolithographic step was performed. Alignment marks were made by etching the InGaAs in a 1:1:38 H_2SO_4:H_2O_2:H_2O solution. Source/drain implants were then performed using photoresist as an implant mask, as shown in Fig. 2(a). Si^{28+} was implanted at energies of 40, 80, 160, and 240 KeV with doses of 4.5×10^{13}, 9×10^{13}, 1.5×10^{14}, and 3×10^{14} cm^{-2}, respectively. Multiple implants were performed in order to achieve a uniform silicon concentration of 2×10^{19} cm^{-3} to a depth of 0.2 μm as determined from LSS statistics. After stripping the photoresist, a second photolithographic step was performed and the channel was implanted at energies of 40, 80, 160, and 240 keV with doses of 1.6×10^{12}, 3.2×10^{12}, 6.3×10^{12}, and 1×10^{13} cm^{-2}, respectively. Multiple implants were again performed in

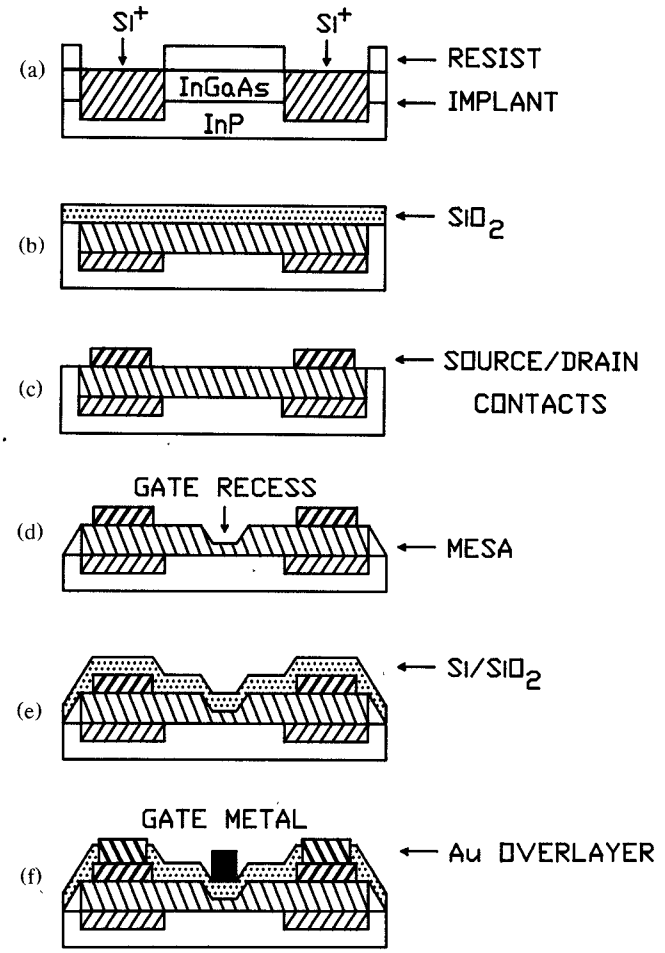

Fig. 2. Fabrication process cross sections for InGaAs MISFET with silicon/silicon dioxide gate insulator.

order to obtain a concentration of at least 10^{17} cm^{-3} to a depth of 0.35 μm.

After stripping the photoresist, the wafer was again cleaned and then encapsulated with silicon dioxide plasma deposited to a thickness of about 1400 Å, as shown in Fig. 2(b) [18]. The implants were than subjected to rapid thermal annealing at 700°C for 30 s in a hydrogen (H_2) ambient. The H_2 flow rate was 2 l/min. After stripping the oxide, source/drain ohmic contacts were defined by evaporating Au/Ge 12 wt.% eutectic and Au to a thickness of 2000 Å and 1500 Å, respectively, and using a lift-off process, as shown in Fig. 2(c). Ohmic contacts were obtained by alloying for 5 min at 400°C in forming gas (10% H_2/N_2). A mesa etch was then performed for device isolation using a 1:1:38 H_2SO_4:$H_2O_2H_2O$ solution. The gate region was then chemically recessed as shown in Fig. 2(d), using a 1:1:100 H_2SO_4:H_2O_2:H_2O solution.

After stripping the photoresist, the wafer was again cleaned and a silicon dioxide gate insulator with a silicon interfacial layer was plasma deposited to a thickness of about 900 Å, as shown in Fig. 2(e) [18]. The films were deposited using a Technics PlanarEtch IIA plasma system modified for 13.56 MHz operation. The silicon interfacial layer was deposited at a pressure of 105 mtorr using 10 W of RF power, a SiH_4 flow rate of 17.5 sccm, and a substrate temperature of 250°C. The silicon dioxide films were deposited at 350 mtorr and 250°C using a 50 W plasma. The SiH_4 and N_2O flow rates were 19 sccm and 55 sccm, respectively. The gate insulators were subsequently annealed at 300°C for 30 min in hydrogen.

The gate metal was then defined by evaporating Ti and Au to a thickness of 300 Å and 4000 Å, respectively, and using a lift-off process. Finally, source/drain oxide windows were opened and an Au overlayer was deposited to a thickness of 4000 Å using a lift-off process, as shown in Fig. 2(f). The Au overlayer assisted the current handling of the devices and facilitated wire bonding to the drain regions.

The InGaAs MISFET's with silicon/silicon dioxide gate insulators were prepared for RF packaging by first thinning the back side using a (10:1:1) HCl:HNO_3:H_2O solution to improve thermal resistance and then scribing the sample into individual MISFET's. Back-side metalization was then performed to aid heat dissipation of the MISFET's by evaporating Ti and Au to a thickness of 300 Å and 4000 Å, respectively. The completed MISFET's were then packaged and wire bonded for microwave characterization at 9.7 GHz.

III. Results

A photograph of a fabricated InGaAs MISFET with a 1 mm total gate width is shown in the upper diagram of Fig. 3. The $I-V$ characteristics of an InGaAs MISFET with a silicon/silicon dioxide gate insulator are shown in the lower diagram of the figure. The gate width of the device is 200 μm. The horizontal scale is 0.5 V/division and the vertical scale is 20 mA/division. The gate voltage step is -2 V. At a drain–source voltage of 4 V, the drain saturation current was 105 mA. The transconductance was typically about 20 mS/mm. The devices had typical source–drain breakdown voltages of 5–7 V. Only a very slight hysteresis was present in the $I-V$ curves. In addition, complete pinch-off of the drain current was not achieved in a manner similar to that observed by other workers [8], [9], [11]. The lack of dc pinch-off may be due to the formation of an inversion layer, which screens the undepleted channel from further gate control [8], [11]. At microwave frequencies, however, this phenomenon is not expected to degrade device performance.

Fig. 4 shows the output power and power-added efficiency as a function of input power from 22 dBm to 26 dBm for a 1-μm-gate-length InGaAs MISFET with a total gate width of 1 mm. The measurements were performed at a frequency of 9.7 GHz using a gate–source bias of 0 V and a drain–source bias of 5 V. The device saturation current density was 770 mA/mm of gate width. An output power density of 1.07 W/mm of gate width was obtained with a corresponding power gain and power-added efficiency of 4.3 dB and 38%, respectively, for an input power of 26 dBm. To our knowledge, this is

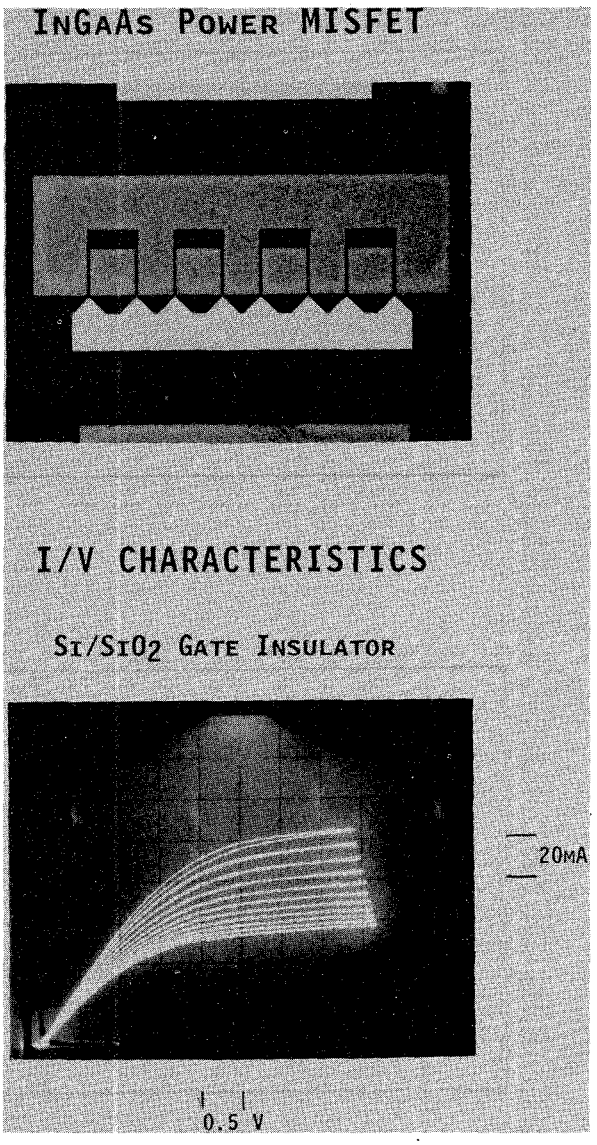

Fig. 3. *Upper diagram*, Photograph of fabricated InGaAs MISFET with 1 mm total gate width; *lower diagram*, $I-V$ characteristics of InGaAs MISFET with silicon/silicon dioxide gate insulator. Horizontal: 0.5 V/div. Vertical: 20 mA/div. Gate (V_{gs}): -2 V/step.

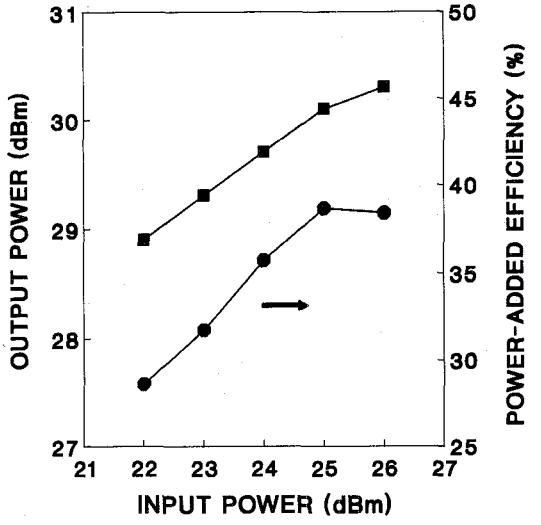

Fig. 4. Output power and power-added efficiency versus input power at 9.7 GHz ($V_{ds} = 5$ V, $V_{gs} = 0$ V).

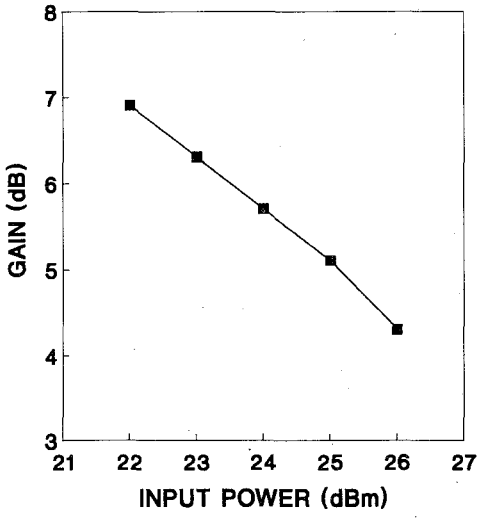

Fig. 5. Power gain versus input power at 9.7 GHz ($V_{ds} = 5$ V, $V_{gs} = 0$ V).

the first demonstration of an output power greater than 1 W for an InGaAs-based transistor on InP. The highest power-added efficiency obtained was 40% with a corresponding power gain and output power density of 4.8 dB and 0.96 W/mm, respectively, at a drain–source bias of 4.5 V and an input power of 25 dBm.

Variation of power gain as a function of input power in the range of 22 dBm to 26 dBm is illustrated in Fig. 5. The gate-source bias and drain–source bias were 0 V and 5 V, respectively. The power gain decreases with an increase in input power, indicating that the device is operating in compression. At an input power of 22 dBm, the power gain was 6.9 dB, with a corresponding output density and power-added efficiency of 0.78 W/mm and 29%, respectively. As the input was increased to 26 dBm, the power gain decreased to 4.3 dB.

In addition, the drain bias current decreased from 432 mA to 330 mA as the microwave input power was increased from 22 dBm to 26 dBm. This effect arises from the nonlinearity of the device $I-V$ characteristics at positive gate voltages when the device is operated under large-signal conditions in compression. Large positive RF signal excursions are not as effective in varying the drain current as large negative signal excursions. Thus, as the RF input power is increased, the drain bias current decreases on the average.

Results were not obtained at lower input powers because the devices display a burnout phenomenon similar to that described previously for InP power MISFET's of comparable geometry [14]. As described above, the drain current increases with a decrease in input power. In order to apply sufficient drain bias voltage to yield high output power, a minimum input power level must be applied to keep the drain current low enough to prevent a destruc-

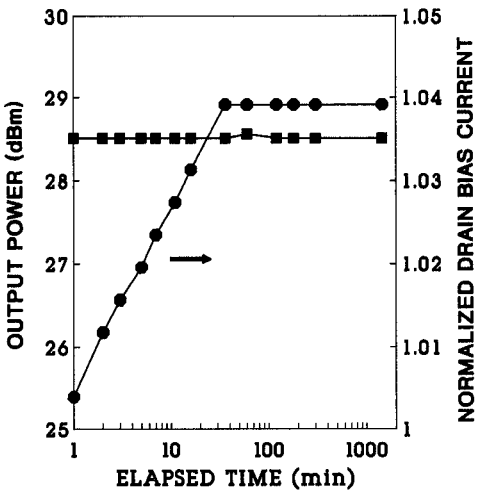

Fig. 6. Time dependence of output power and drain bias current.

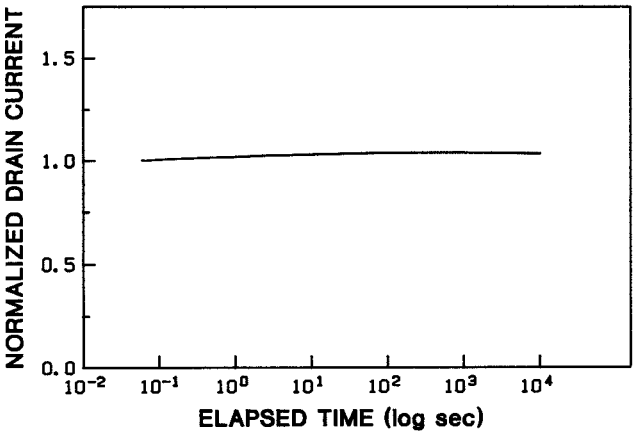

Fig. 7. Drain current drift measurement of InGaAs MISFET with silicon/silicon dioxide gate insulator.

tive thermal breakdown. Therefore, the input power range is restricted to regions that drive the device into compression.

Fig. 6 illustrates the output power and normalized drain bias current (I_{ds}/I_{ds0}) variation of a representative 1-mm-gate-width device over a 24 h period. The RF input power, drain–source bias voltage, and gate–source bias voltage were held constant at 25 dBm, 4.8 V, and −5 V, respectively. The measurement frequency was 9.7 GHz and the initial drain bias current (I_{ds0}) was 256 mA. The output was stable to within 1.2%, and the drain bias current increased less than 4% over 24 h of continuous operation. To our knowledge, this is the first report of RF output power stability measurements on InGaAs MISFET's.

The results of the drain current drift measurement of an InGaAs MISFET with a 200 μm gate width and a silicon/silicon dioxide gate insulator are shown in Fig. 7. The drain–source bias was 2.5 V. The gate–source bias was initially 0 V and the drain current was 84.3 mA. Immediately prior to the start of the drift measurement, the gate–source bias was switched to −5 V, which reduced the drain current to 57.5 mA. Thus, during the entire drift measurement, the channel was partially depleted, with the drain current at approximately 70% of its zero-gate-bias value. The drain current increased only 4% over a period of 10^4 s. The general trend of the data indicates an initial increase in drain current over the first 350 s followed by a decrease toward the initial drain current value. The fact that the drain current can be held at a reduced level with negative gate bias under strictly dc conditions is an important result which reflects the potential usefulness of the devices. The results indicate that the devices can be maintained in a partially pinched condition over extended time periods and, thus, provide a potential solution to the RF burnout phenomenon described above.

IV. Summary

Depletion-mode InGaAs MISFET's with 1 μm gate lengths were fabricated using an ion-implanted process. A plasma-deposited silicon dioxide gate insulator with a thin silicon interfacial layer was used as the gate insulator. At 9.7 GHz, a 1-mm-gate-width device produced an output power of 1.07 W with a corresponding power gain and power-added efficiency of 4.3 dB and 38%, respectively. The highest power-added efficiency was 40% at 0.96 W output power and 4.8 dB gain. The output power was stable to within 1.2% over 24 h of continuous operation, with a corresponding drain bias current increase of less than 4%. This is the first report of RF power measurements on an InGaAs MISFET with a silicon/silicon dioxide gate insulator. In addition, RF output greater than 1 W has been demonstrated for the first time for an InGaAs-based transistor on InP. Also, using strictly dc gate bias voltage (i.e., with no RF signal present), device drain current was held at approximately 70% of its zero-gate-bias value over a period of 10^4 s with only a 4% drift. The capability to partially pinch off the device under strictly dc conditions may provide a solution to the burnout problem observed in these devices when the RF signal is removed while holding the device at high drain bias voltage. Further improvements are expected by optimizing the device structure. Enhanced frequency performance is expected through the use of submicron gate lengths.

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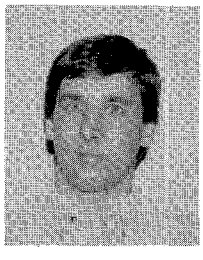

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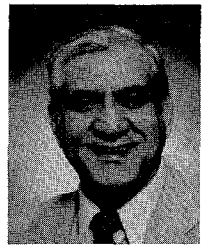
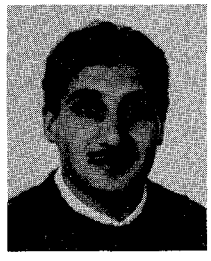
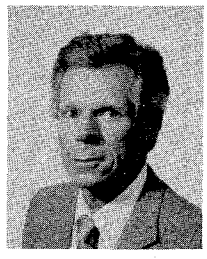


Vik J. Kapoor (S'75–M'76–SM'83) received the M.S. and Ph.D. degrees in 1972 and 1976, respectively, from Lehigh University.

He was a Senior Engineer and a member of the technical staff at Fairchild Semiconductor, Palo Alto, CA, from 1976 to 1978. In 1978 he joined the faculty of the Case Western Reserve University, where he was the Director of the Solid State Integrated Circuits Laboratory until 1983. He is presently a Professor and Head of the Electrical and Computer Engineering Department at the University of Cincinnati. His research focuses on compound semiconductor technology including heterostructures and quantum well devices for the next generation of high-power, high-frequency devices for applications in microwave and digital integrated circuits. He is also investigating high-temperature superconductors for passive and active microelectronic devices for microwave applications.

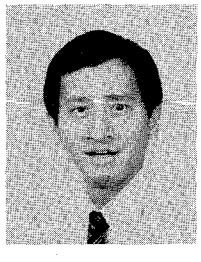


Mohsen Shokrani received the B.S. degree in physics in 1986 from Thomas More College, Fort Mitchell, KY. He then joined the Electrical Engineering Department at the University of Cincinnati, where he received the M.S. degree in electrical engineering. His thesis research was on the development and characterization of novel gate insulators for InP and InGaAs power MISFET fabrication. He is currently pursuing the Ph.D. degree at the University of Cincinnati. His dissertation research is on InGaAs transistors for microwave and millimeter-wave monolithic integrated circuit applications in switches and phase shifters.



Louis J. Messick received the B.S. and M.S. degrees in physics from San Diego State College, San Diego, CA, in 1964 and 1967, respectively, and the Ph.D. degree in solid-state physics from the University of California, Santa Barbara, in 1972. His graduate work was in the area of direct and modulation UV spectroscopy of transition metal compounds.

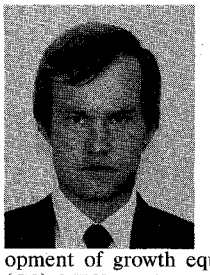
Since 1972 he has worked as a Research Physicist at the Naval Ocean Systems Center, San Diego, CA, where his area of research and development has been III–V semiconductor devices and circuits for high-speed and optoelectronic as well as microwave and millimeter-wave power applications.



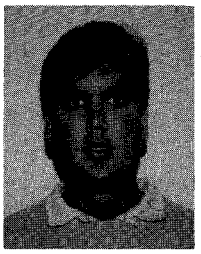
Richard Nguyen (M'82) was born in Saigon, South Vietnam, in 1958. He received the B.S. degree in electrical engineering in 1982 from the University of Hawaii, Honolulu.

From 1982 to 1985 he was with the semiconductor research and development laboratories of the Motorola Corporation, where he was involved in all phases of GaAs technology development. Since 1985, he has worked as a device process development engineer at the Naval Ocean Systems Center, San Diego, CA, where he has been engaged in research on compound semiconductor devices and circuits for high-power, high-speed, and optoelectronic applications.

Richard A. Stall received the B.S. degree from the California Institute of Technology in 1977 and the Ph.D. degree in electrical engineering in 1980 from Cornell University.



He was a member of the technical staff at AT&T Bell Laboratories, Murray Hill, NJ, for four years and was responsible for the development of MBE technology for optoelectronic devices. His research resulted in the development of low-threshold semiconductor lasers and high-frequency heterojunction bipolar transistors. He is currently Vice President, Systems Technology, at the Emcore Corporation, Somerset, NJ. His work involves the development of growth equipment and processes for MOCVD, gas source (GS) MBE, and vapor transport epitaxy (VTE) of III–V and II–VI compounds.



Mark A. McKee (S'86–M'86) was born in St. Petersburg, FL, in 1963. He received the B.S. degree in materials science engineering in 1986 from the University of Florida, Gainesville. He is currently pursuing the M.S. degree in materials science at Rutgers University, NJ.

Since 1986 he has worked as a material science engineer at the Emcore Corporation, Somerset, NJ. His area of research has been in MOCVD in the process development and characterization of various types of III–V devices, among them high-quality visible lasers, quaternary lasers, and photodetectors.